Scheme – G

Sample Test Paper-I

Course Name : Electronics Engineering Group

Course Code : EJ/EN/ET/EX/EV/IC/IE/IS/MU/DE/ED/ET/IU

17320

Semester : Third

Subject Title : Principles of Digital Techniques

Marks : 25 **Times:1 Hour**

Instructions:

1. All questions are compulsory.
2. Illustrate your answers with neat sketches wherever necessary.
3. Figures to the right indicate full marks.
4. Assume suitable data if necessary.
5. Preferably, write the answers in sequential order.

Q1. Attempt any THREE of the following. **09 Marks**

a. Write truth table of Substractor.

b. Find Binary multiplication of $(110101)_2$ * $(101001)_2$

c. Implement following expression using MUX.
$F(A,B,C,D) = \Sigma m\ (1,2,3,5,7,9,12)$

d. Draw the circuit diagram of CMOS – NOT gate.

Q2. Attempt any TWO of the following. **08 Marks**

a. State and prove De-Morgan's theorem.

b. Find BCD subtraction using 10's compliment for the following.
1. $(95)_{10} - (62)_{10}$
2. $(15)_{10} - (45)_{10}$

c. Minimize the following expression using K-map.
$F(A,B,C,D) = \Sigma\ m\ (1,2,3,5,6,7,9,13,15)$

Q3. Attempt any TWO of the following. **08 Marks**

a. Prove $(A+\overline{B}+AB)\ (A+\overline{B})\ \overline{A}\ B=0$ with help of Boolean Laws

b. Convert the following Binary code into Excess-3 and Gray code.
1. $(10110.101)_2$
2. $(111101001)_2$

c. Give any Four Characteristics of ECL Family.

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Sample Test Paper-II

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Course Code : EJ/EN/ET/EX/EV/IC/IE/IS/MU/DE/ED/ET/IU

17320

Semester : Third

Subject Title : Principles of Digital Techniques

Marks : 25 **Times:1 Hour**

Instructions:

1. All questions are compulsory.
2. Illustrate your answers with neat sketches wherever necessary.
3. Figures to the right indicate full marks.
4. Assume suitable data if necessary.
5. Preferably, write the answers in sequential order.

Q1. Attempt any THREE of the following. **09 Marks**

a. Define modulus of a counter? Draw Block Diag. of IC 7490.
b. Compare combinational and Sequential logic circuit.
c. Desribe Decimal to BCD priority Encoder
d. Compare Weighted resistor method and R-2R method of DAC types

Q.2 Attempt any TWO **08 Marks**

a. Describe Dual slope ADC with Diagram.
b. Describe Master Slave JK flip flop with Diagram
c. Compare
1) Static RAM and Dynamic RAM.
2) Volatile and Non-Volatile Memory.

Q.3 Attempt any TWO **08 Marks**

a. Draw 4 bit SIPO shift Register using D Flip flop. Explain its working.
b. Describe with Diagram Binary weighted Resistor DAC. Derive it's output expression.
c. Draw D and T Flip-Flop using JK Flip Flop.

Scheme – G

Sample Question Paper

Course Name : Electronics Engineering Group

Course Code : EJ/EN/ET/EX/EV/IC/IE/IS/MU/DE/ED/ET/IU

17320

Semester : Third

Subject Title : Principles of Digital Techniques

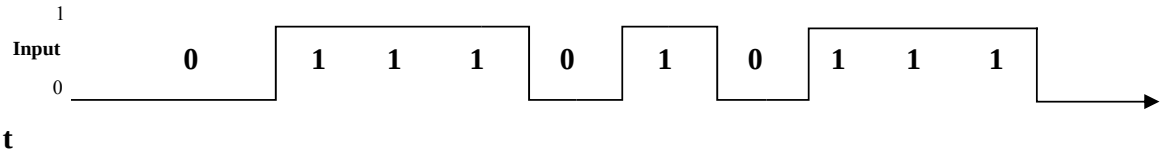
Marks : 100 **Time: 3Hrs.**

Instructions:

1. All questions are compulsory
2. Illustrate your answers with neat sketches wherever necessary
3. Figures to the right indicate full marks
4. Assume suitable data if necessary
5. Preferably, write the answers in sequential order

Q1 A. Attempt any SIX **20 marks**

a. Define Excess-3 code and find Excess-3 code of 101,1011 binary
b. Describe MUX with help of Truth
c. Define Modulus of the counter
d. List the various types shift registers
e. State Parameters of DAC
f. Identify the IC 2716 and 6116.
g. State AND laws
h. Find the output waveform of NOT gate (Inverter) for the following input waveform



Q1 B. Attempt any TWO **08 Marks**

a. Describe Hexadecimal , Octal Number system
b. Minimize the following using K-map.
F (A, B, C) = π M (0, 1, 2, 3, 7)
c. Implement the following Boolean function using a 3:8 decoder and external gates
F(A,B,C) = ∑ (1,2,3,5,6,7)

Q2. Attempt any FOUR **16 Marks**

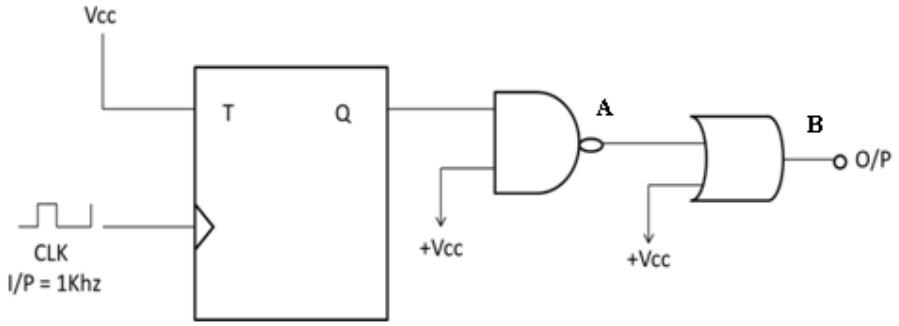
a. Convert the following decimal into binary, hexadecimal $(268)_{10}$ $(49.25)_{10,}$
b. Implement function of OR using NAND

c. Describe 4 variable K-Map reduction rules
d. Define triggering methods
e. Draw & explain IC 7490 as mod 6
f. Draw the circuit diagram of 4 bit R-2R ladder DAC write its output voltage expression

Q3. Attempt any FOUR **16 Marks**

a. Write the logical expression of conversion Binary to Gray code using K-Map
b. State difference between TTL & CMOS
c. Draw internal logic diagram of Bidirectional Buffer IC 74245 & Explain its operation

d. Draw the output waveforms at point A and at point B for the circuit given the fig.



Assume clock input frequency of 1 kHz,

e. Describe with circuit diagram Successive Approximation Register ADC
f. Explain internal organization of a 16 X 4 Memory chip with suitable diagram

Q4. Attempt any FOUR **16 Marks**

a. Describe the circuit diagram of ECL Family
b. Implement 1:32 DeMux using 1:8 DeMux only
c. What is Race around condition & How it is avoided in JK Flip – flip?
d. Describe operation of 3 bit twisted Ring Counter using JK flip-flop
e. Compare single slope and dual slope ADC
f. Compare Volatile and Non – Volatile Memory

Q5. Attempt any FOUR **16 Marks**

a. Explain the circuit of CMOS NOT gate
b. Define Priority Encoder? Explain Octal to Binary Priority Encoder
c. Describe steps to construct a circuit of 3bit Synchronous Counter.
d. Describe to construct a Mod 5 ripple counter using 3 bit ripple counter
e. Draw the block diagram of single slope ADC and explain its working
f. Draw and explain Diode Matrix ROM for 8 x 8 array.

Q6. Attempt any FOUR **16 Marks**

a. Solve 1101 -1001 using 1's and 2's complement
b. State and prove DeMorgans theorems
c. Describe steps to construct a Single Digit BCD adder using IC 7483
d. Describe steps to construct a 32:1 MUX using 4:1 MUX

e. Describe working of 4 bit asynchronous Up-Down counter

f. Find output voltage V_0 for following inputs-

1) $(0101)_2$
2) $(1100)_2$

Given A 4 bit DAC generates output Voltage $V_0 = 2v$ for Digital input of $(0010)_2$
